Exhibit 15

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COMMITTEE LETTER BALLOT
Item # 2129.04

SUBJECT: DDR2 RDIMM Specification Revision 3.91 for Raw Card M supporting up to 1Gb SDRAM.

BACKGROUND: Previous R/C M design does not support up to 1Gb SDRAM since BA2 had not been wired.
A modified R/C M design proposal was shown to JC45.1 in March 2007 and the committee authorized the 4 Rank. RDIMM TG to issue design spec revisions and registration ballot.
4R DIMM TG agreed by e-mail consensus vote to ballot R/C M design spec changes on 5/06/2007.

The object of this ballot is R/C M.

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KEYWORDS & ACRONYMS:
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Exhibit
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PC2-6400/PC2-5300/PC2-4200/PC2-3200
Registered DIMM Design Specification

Revision 3.91

April 26, 2007

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4 Rank RDIMMs:

DDR2 Registered DIMMs with 4 ranks of memory per RDIMM (raw cards M and N) are a recent addition to the DDR2 RDIMM family. As such, system designers and users need to be aware of some distinguishing characteristics of these designs.

Product Label:

The 4 rank DDR2 RDIMMs are distinguished on the module label in the “eRxff” field, where e=4. For example, a 4GB 4 rank RDIMM built using x4 SDRAMs would be labeled:

- **4GB 4Rx4 PC2-...**

In addition, the raw card reference design letter field “-ef” will indicate the standard design used, if any. For example, a complete label example for such an RDIMM based on raw card M revision 0 with address parity and SPD version 1.2 using DDR2-533 SDRAMs with CAS latency, tRCD, and tRP of 4 clocks each would be:

- **4GB 4Rx4 PC2-4200P-444-12-M0**

Bus Loading:

Loading on the address and command bus for 4 rank RDIMMs is similar to other raw cards: 1 or 2 loads per signal compared to 1 to 4 loads on other raw cards. Additional pre-register flight time must be accounted for on the $\overline{S}2$ and $\overline{S}3$ signals which require an additional 37 mm of routing on the RDIMM.

DDR2 RDIMMs with 4 ranks place 4 loads on the data bus. For raw card M these are all DQ, CB, DQS, and $\overline{DQS}$ signals. For raw card N these are all DQ, CB, DM, DQS, and $\overline{DQS}$ signals. System simulation must be done to ensure proper operation, especially with systems supporting more than one slot which must verify proper interaction of 4 rank RDIMMs with empty slots or slots containing RDIMMs with 1, 2, or 4 ranks per slot.

Rank Selects, Clock Enables, On-Die Termination:

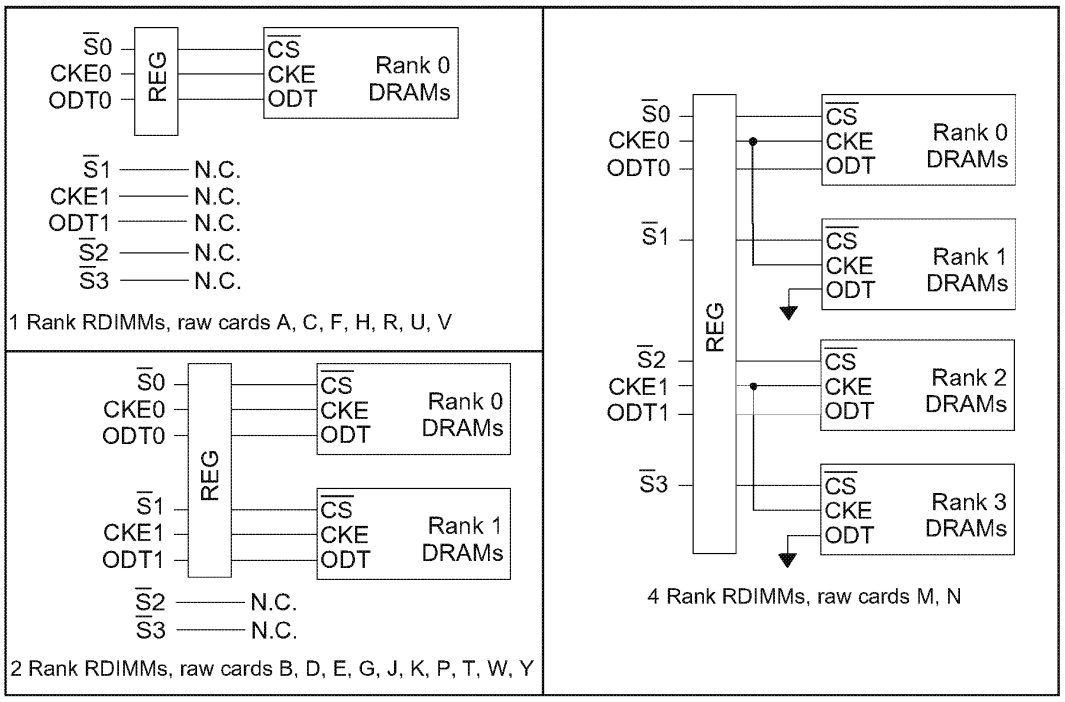
The addition of rank select signals $\overline{S}2$ and $\overline{S}3$ on the motherboard are required in order to support 4 rank RDIMMs. Consistent with the rest of the command and address bus and rank selects $\overline{S}0$ and $\overline{S}1$, it is recommended that routing of rank selects $\overline{S}2$ and $\overline{S}3$ is done referenced to VDD for best signal integrity. All DDR2 RDIMMs (1, 2, and 4 rank versions) reference the data bus, masks, strobes, and clocks to VSS.

Only two clock enable signals, CKE0 and CKE1, and two on-die termination signals, ODT0 and ODT1, are provided at the DDR2 RDIMM edge connector. Controllers must be programmed as appropriate for the following association between signals:

- **$\overline{S}0$ and $\overline{S}1$ associated with CKE0 and ODT0**
- **$\overline{S}2$ and $\overline{S}3$ associated with CKE1 and ODT1**

These associations between control signals are shown graphically in the following block diagrams.

Proposed



Simulation and testing indicate that best signal integrity on the data, mask, and strobe bus is obtained when ODT is programmed for 75 Ω for ranks 0 and 2 of DDR2 SDRAMs via the mode register set command EMRS(1) and both ODT0 and ODT1 RDIMM signals are asserted during cycles requiring termination from the slot containing the 4 rank RDIMM, providing an effective 37.5 Ω termination impedance during these cycles. Since ODT for ranks 1 and 3 are disabled via the ODT pins on these ranks, programming via EMRS(1) is a don't-care for these ranks.

Serial Presence Detect:

Byte 5 of the standard serial presence detect (SPD) describes the number of ranks of memory installed on the RDIMM. A rank of memory is defined as the collection of SDRAMs driven by a given rank select signal, $\overline{S0}$ through $\overline{S3}$. SPD byte 5 of a 4 rank RDIMM will contain the value 0x04.